Amendments to the Claims:

Without prejudice, this listing of the claims replaces all prior versions and listings of the claims in the present application:

Listing of Claims:

1. (Currently Amended) A method for comparing binary data words, comprising:

splitting each of a first data word and a second data word into at least two subwords including one high-order-bit subword and one low–order-bit subword;

comparing the high-order-bit subword of the first data word to the high-order-bit subword of the second data word in a first comparing device to produce a first intermediate comparison result;

comparing the low-order-bit subword of the first data word to the low-order-bit subword of the second data word in a second comparing device to produce a second intermediate comparison result;

applying a control signal to a correction device connected between at least one of the two comparing devices and a logic device; and

gating the two intermediate comparison results in the logic device, depending on the control signal applied to the correction device, wherein an output of the logic device is provided as an overall result;

wherein the overall result is usable for situation-dependent handling in a vehicle system.

2. (Original) The method as recited in claim 1, wherein the two data words are split in a microprocessor system that checks the two data words for agreement, and wherein the logic device is an AND gate.

3. (Original) The method as recited in claim 1, wherein a substitute value, instead of the second intermediate comparison result, is gated with the first intermediate comparison result, dependent on at least one of the control signal and a negative value of the second intermediate comparison result.

4. (Original) The method as recited in claim 3, wherein the control signal is formed by a control unit of a microprocessor, and wherein the substitution of the substitute value instead

of the second intermediate comparison result is dependent on a destination address of the first and second data words to be compared.

5. (Original) The method as recited in claim 3, wherein the control signal is formed by a control unit of a microprocessor, and wherein the substitution of the substitute value instead of the second intermediate comparison result is dependent on instructions in the program code of the microprocessor.

6. (Currently Amended) A system for comparing binary data words, comprising:

a device for splitting each of a first data word and a second data word into at least two subwords including one high-order-bit subword and one low–order-bit subword;

a first comparing device for comparing the high-order-bit subword of the first data word to the high-order-bit subword of the second data word to produce a first intermediate comparison result;

a second comparing device for comparing the low-order-bit subword of the first data word to the low-order-bit subword of the second data word to produce a second intermediate comparison result;

a control device for generating a control signal;

a logic device; and

a correction device connected between at least one of the two comparing devices and the logic device, the correction device receiving the control signal;

wherein the two intermediate comparison results are gated in the logic device, depending on the control signal applied to the correction device, wherein an output of the logic device is provided as an overall result;

wherein the overall result is usable for situation-dependent handling in a vehicle system.

7. (Original) The system as recited in Claim 6, wherein the device for splitting the first and second data words is included in a microprocessor system for checking redundant data words for agreement.

8. (Original) The system as recited in Claim 6, wherein a substitute value, instead of the second intermediate comparison result, is gated with the first intermediate comparison result

in the logic device, dependent on at least one of the control signal and a negative value of the second intermediate comparison result.